
Vicis: A Reliable Network for Unreliable Silicon

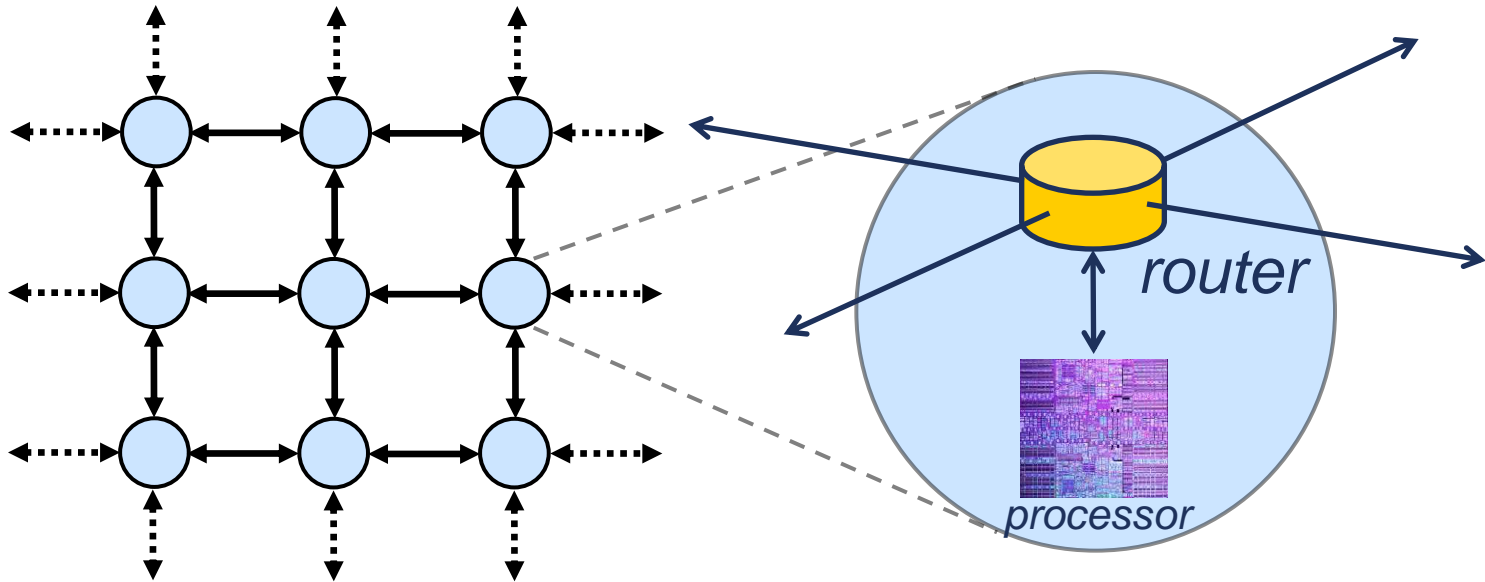
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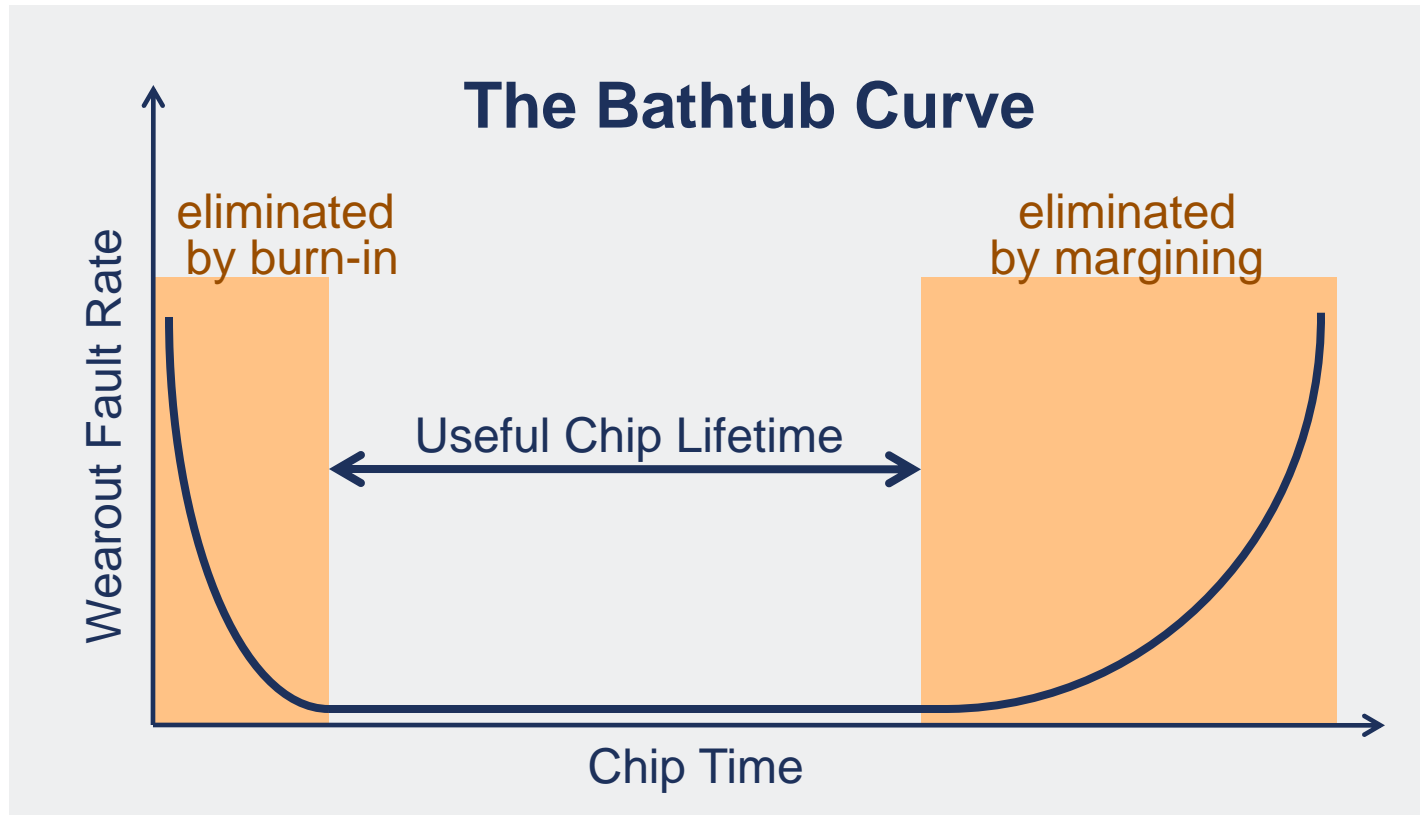
Network-on-Chip

- Growing design complexity → modular architectures
- Network-on-Chip (NoC)
 - Components (processors, memory, etc.) communicate via **routers**
 - Scalable bandwidth, inherent redundancy



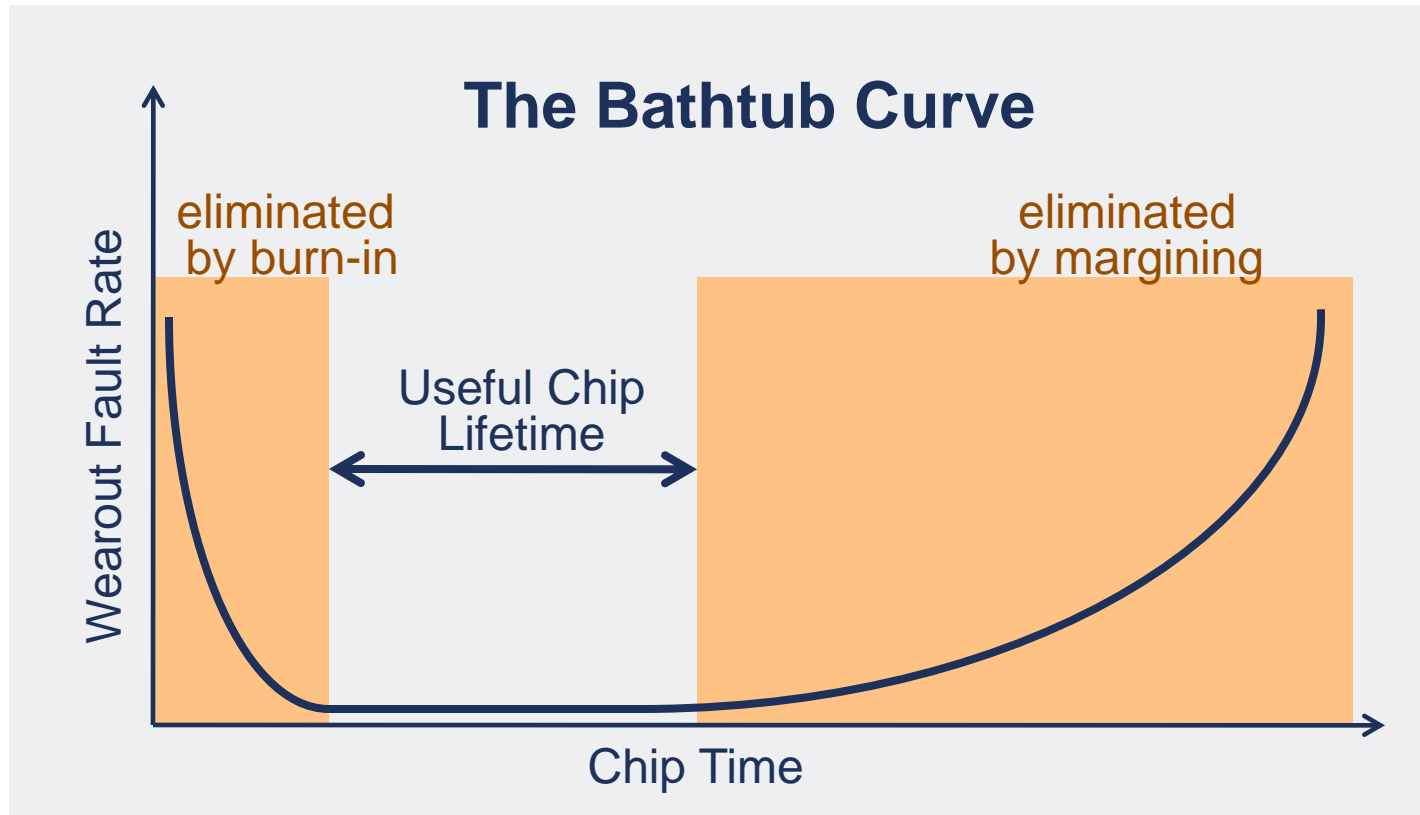
Transistor Wear-Out

- Technology-scaling increases likelihood of wear-out
- Reasons include: oxide breakdown, electromigration, etc.



Transistor Wear-Out

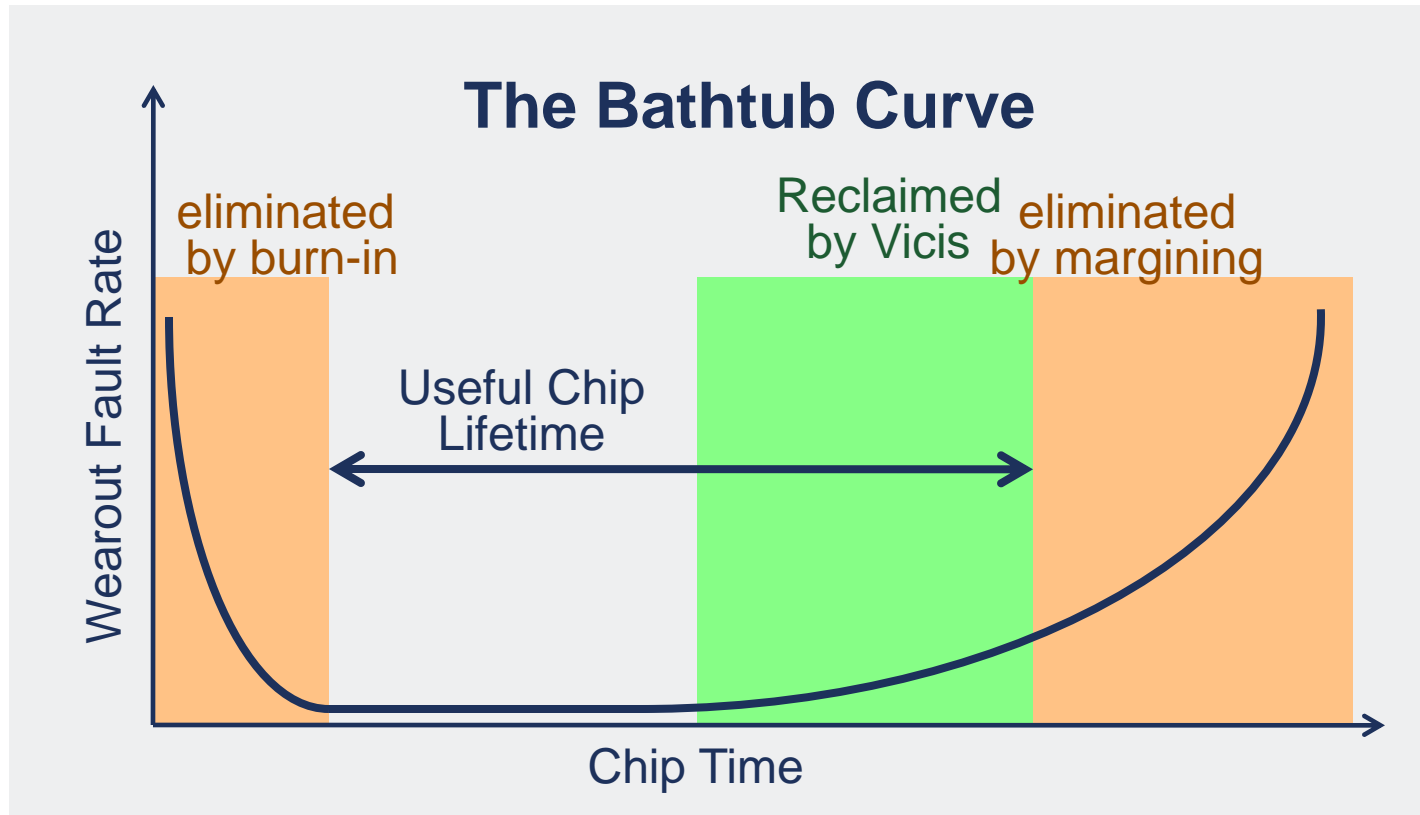
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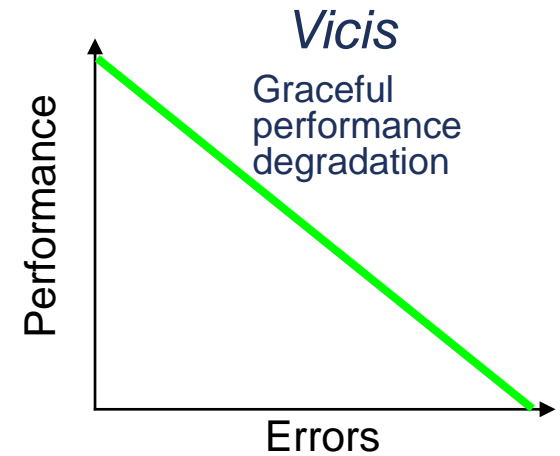
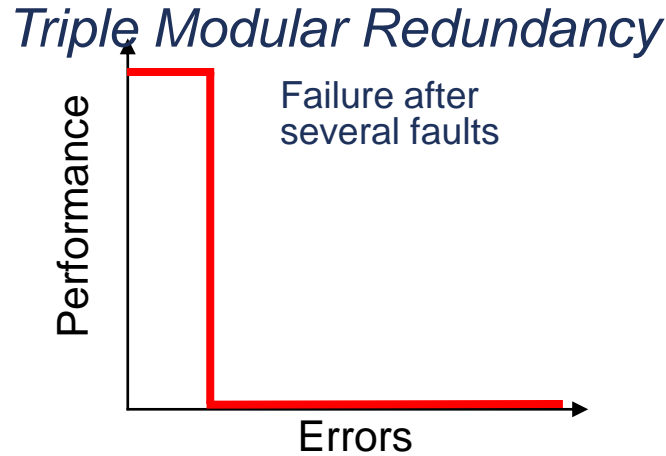
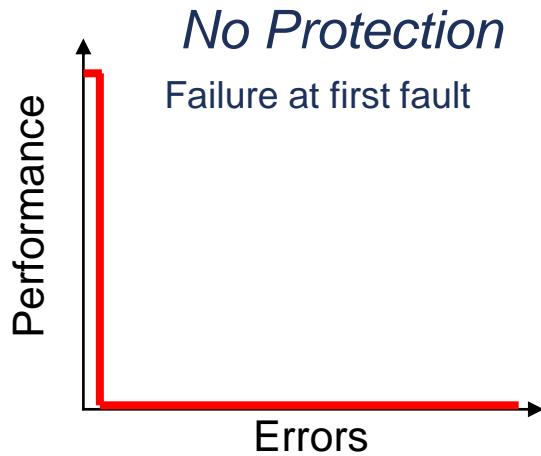
Technology-scaling → shorter useful life

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System Response to Wear-Out

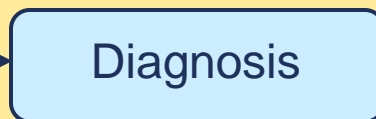


Invariants

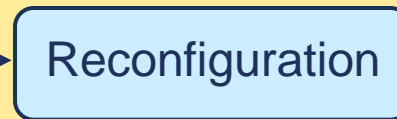


Detect if fault has occurred

Vicis

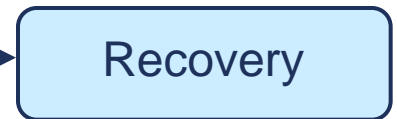


Diagnose what fault has occurred



Reconfigure network to account for fault

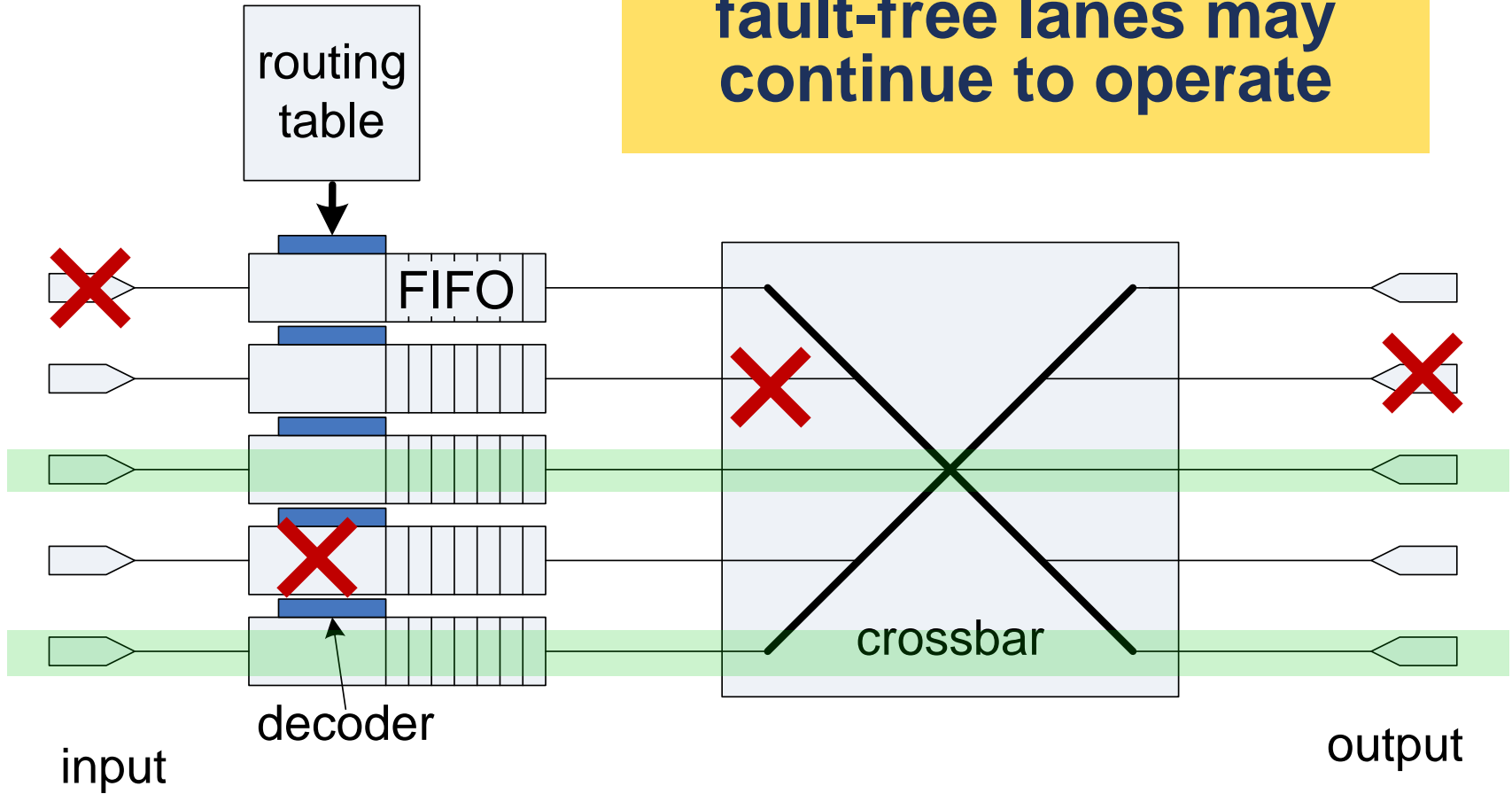
Checkpointing



Recover and resume normal operation

Fault Tolerance Strategy

If faults are isolated, fault-free lanes may continue to operate

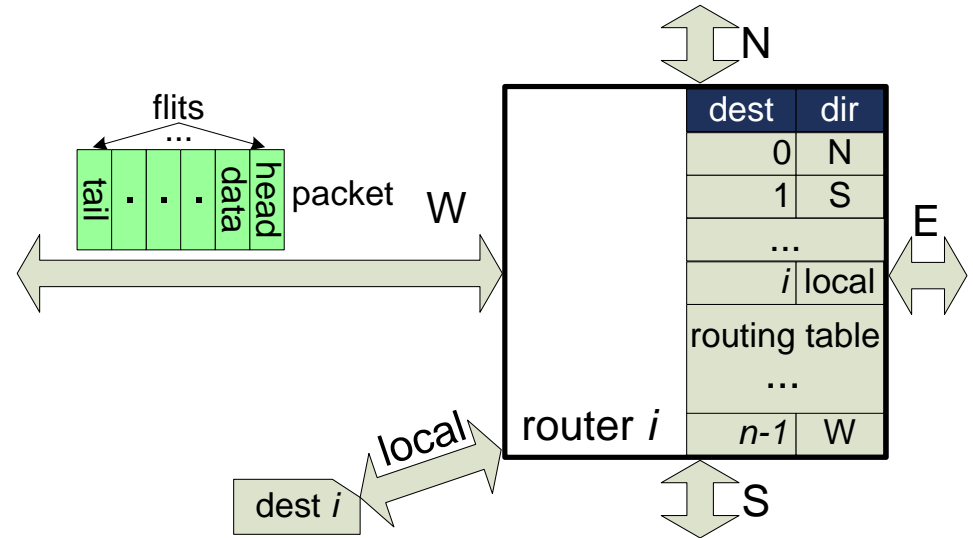


Outline

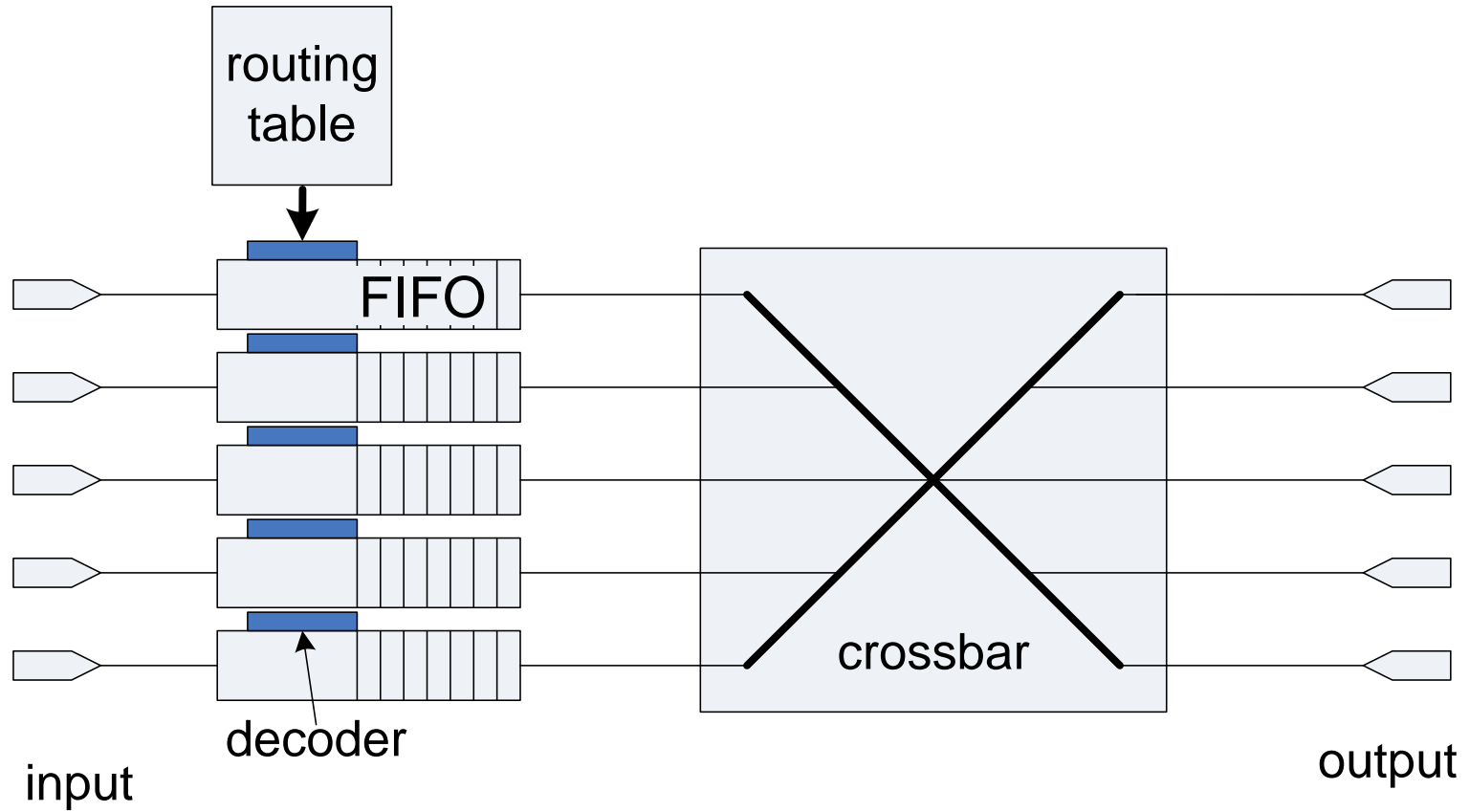
- Architecture Overview
- Diagnostic Approach
- Experimental Results
- Conclusion

Network Assumptions

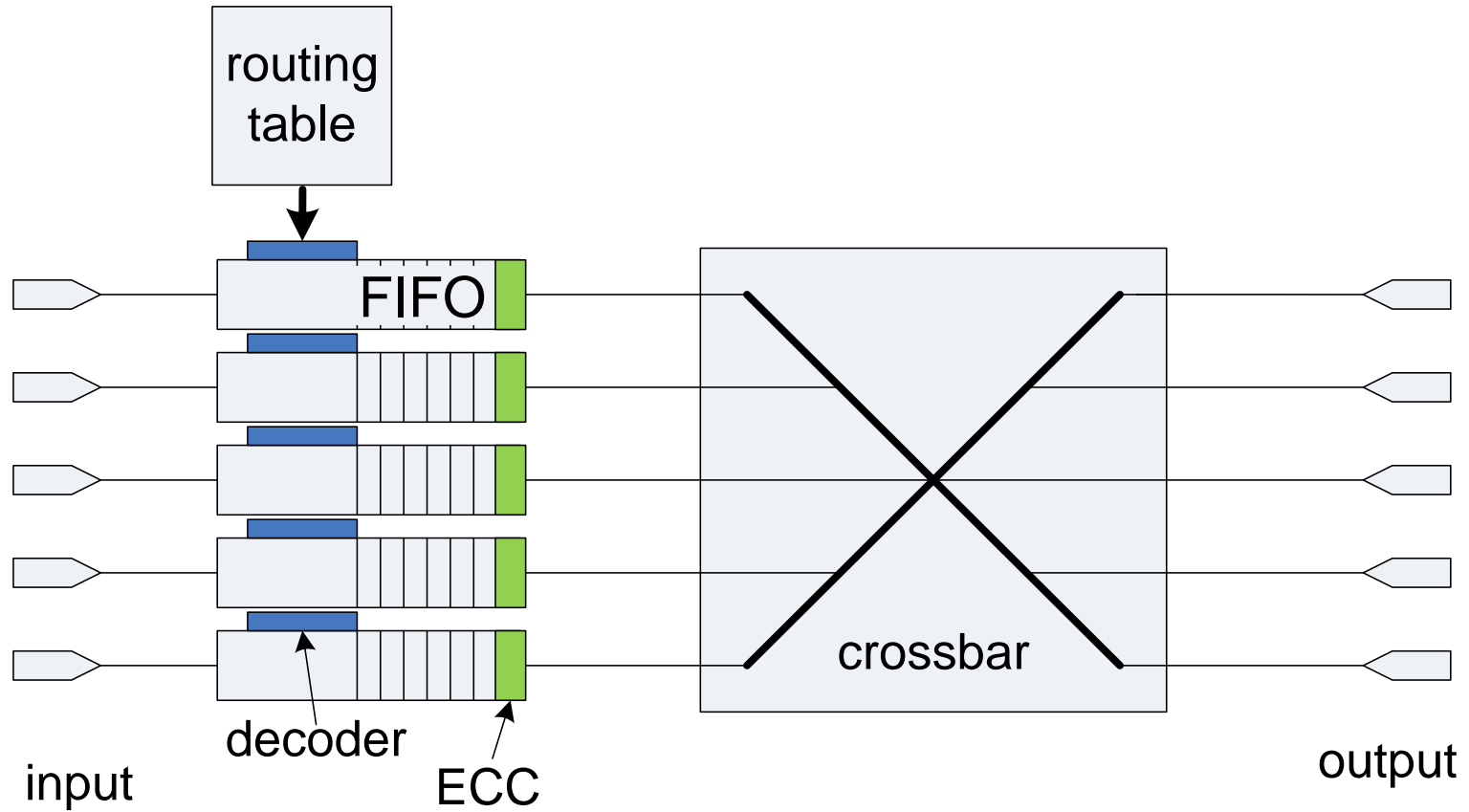
- Wormhole routing
- 2D mesh or torus
- Static routing
- No virtual channels
- Hard fault injection



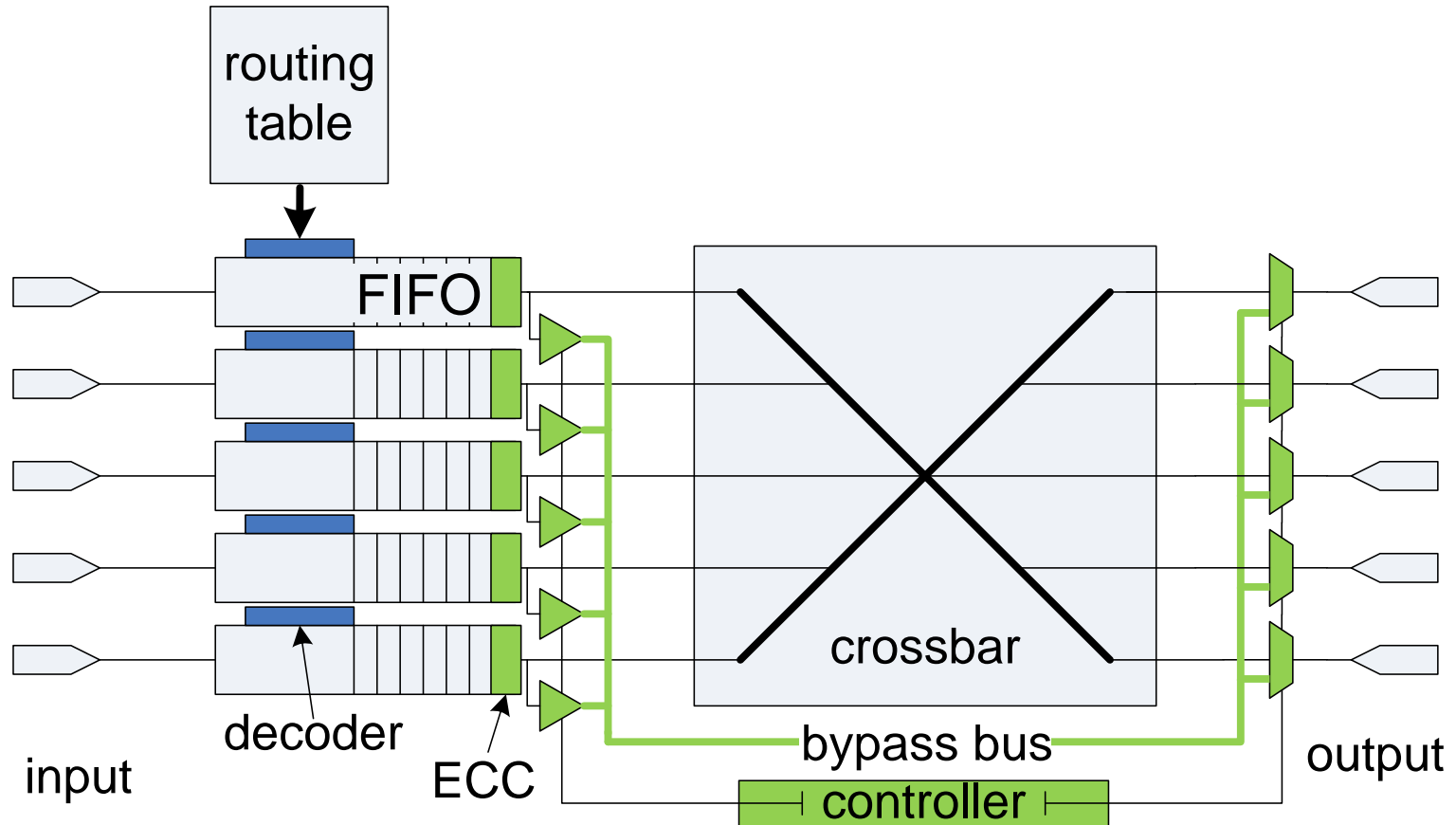
Vicis Reliability Features



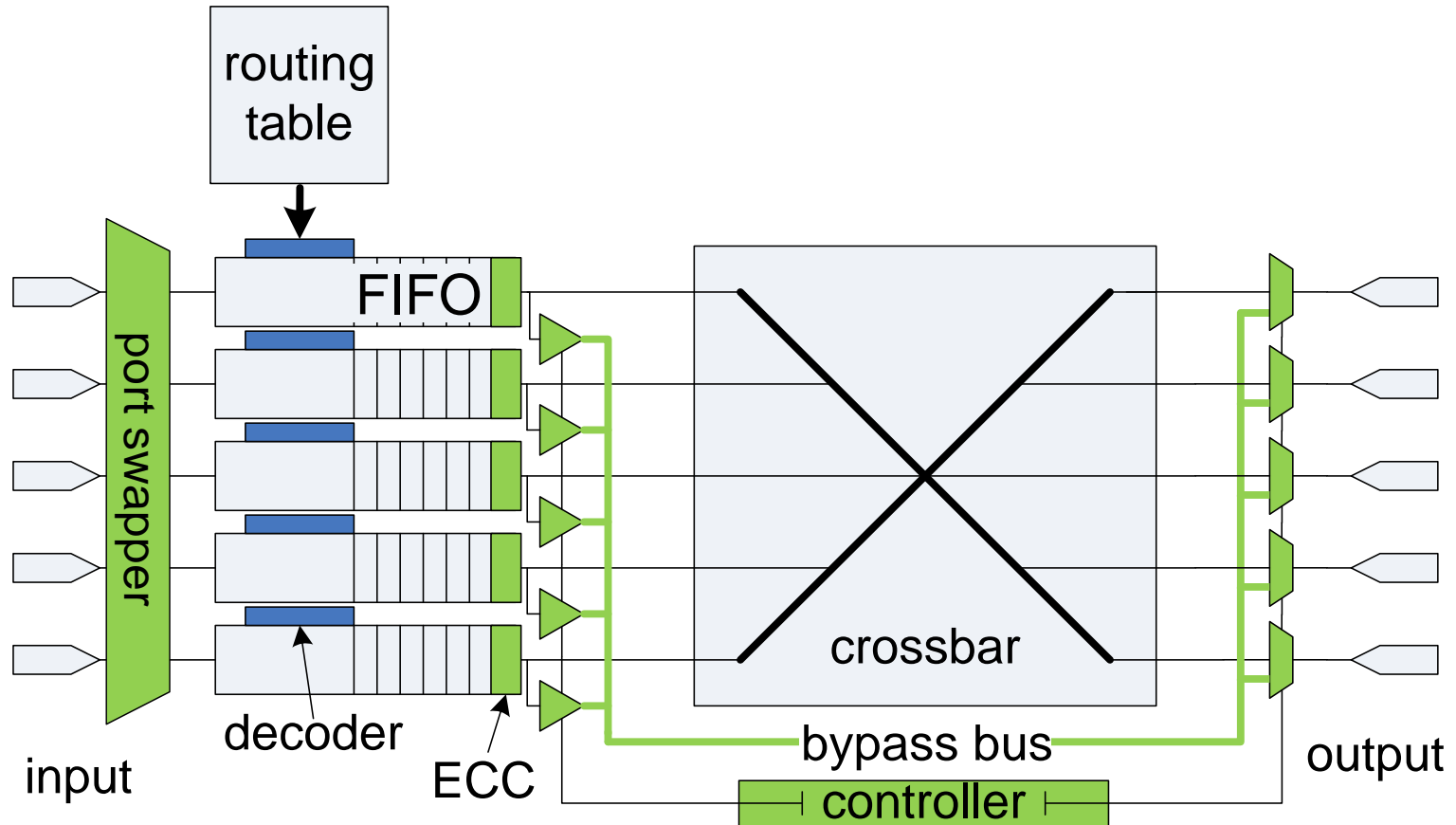
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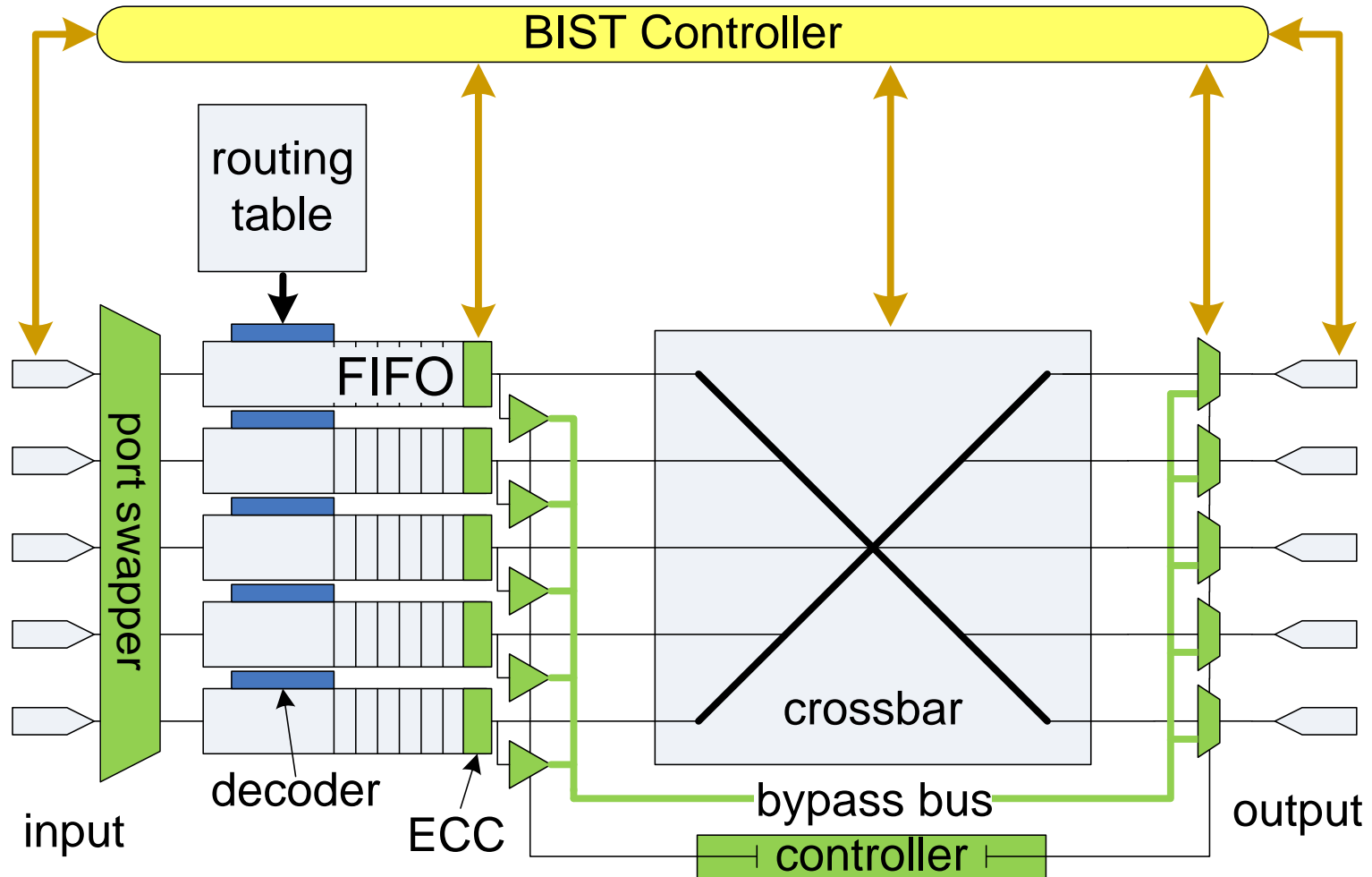
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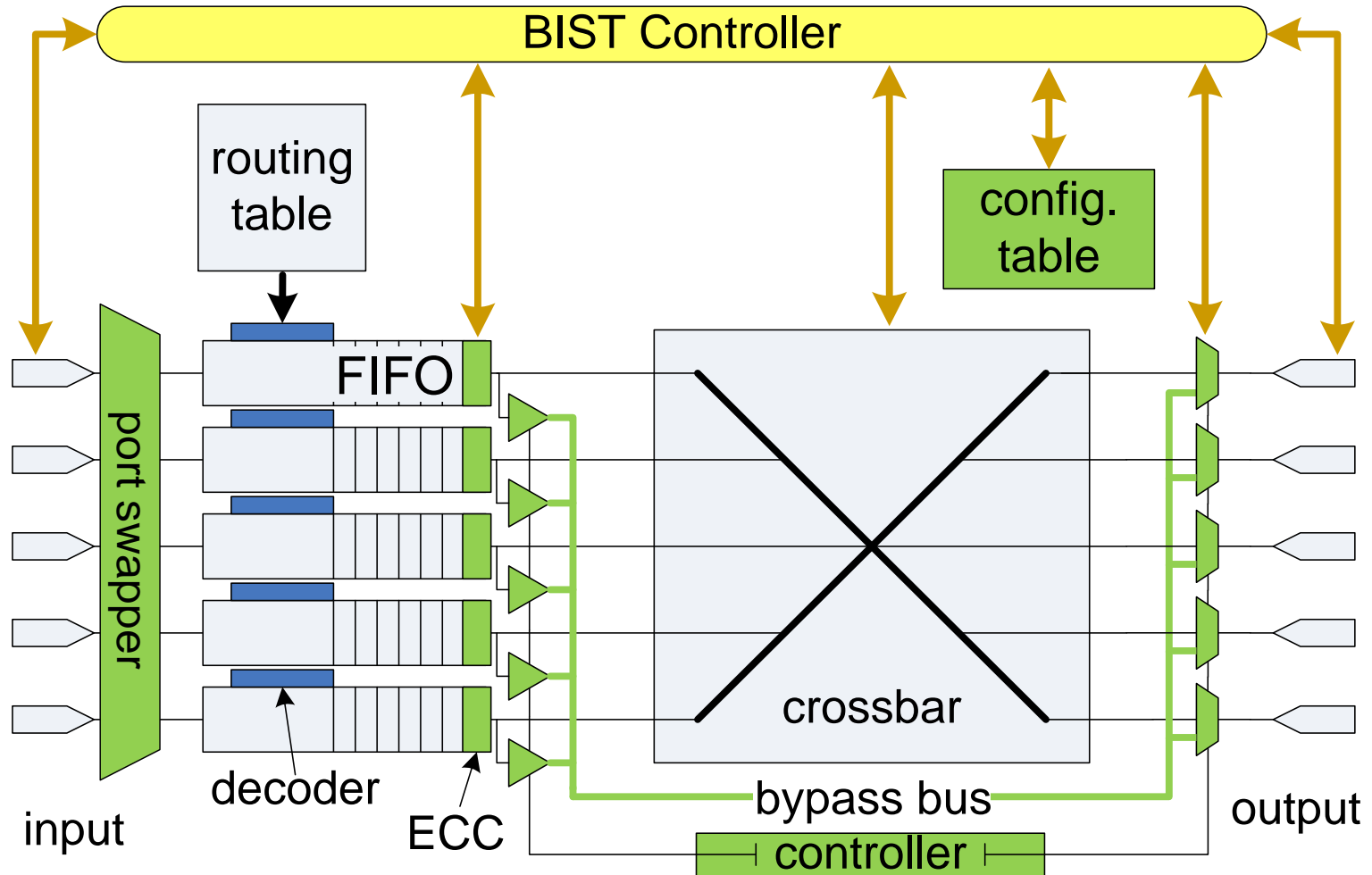
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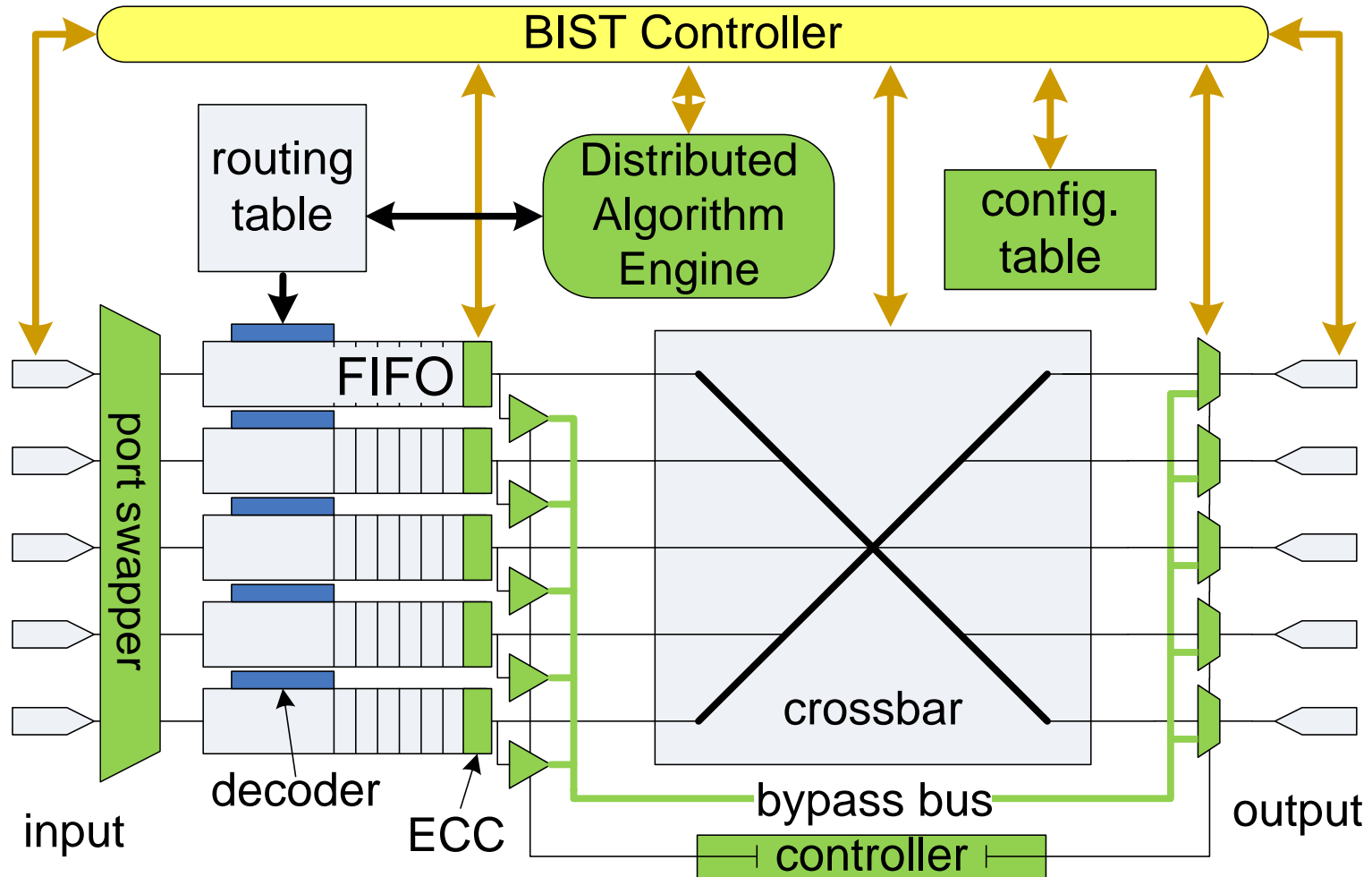
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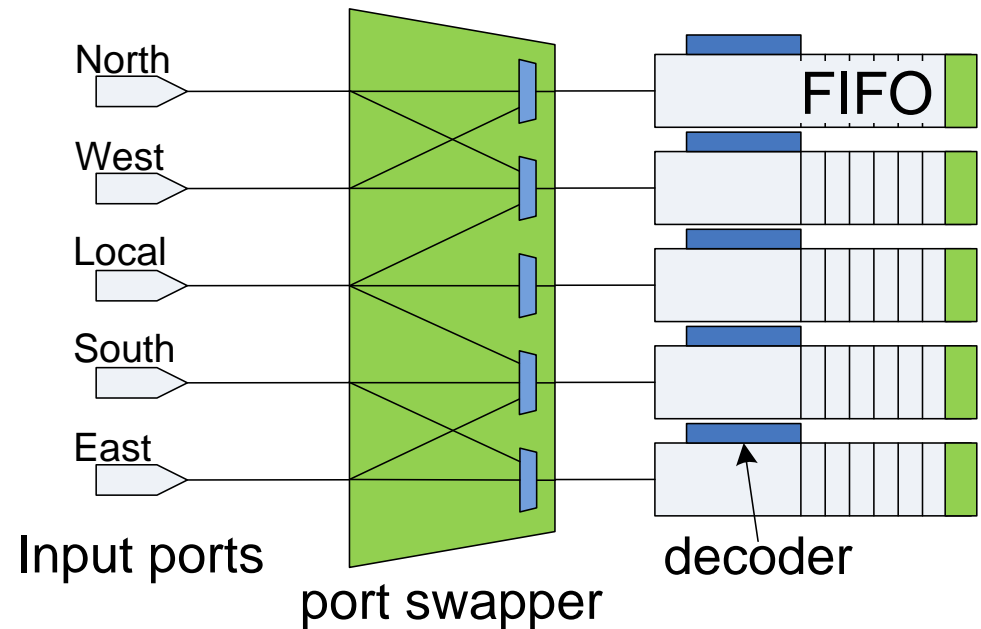


Vicis Reliability Features

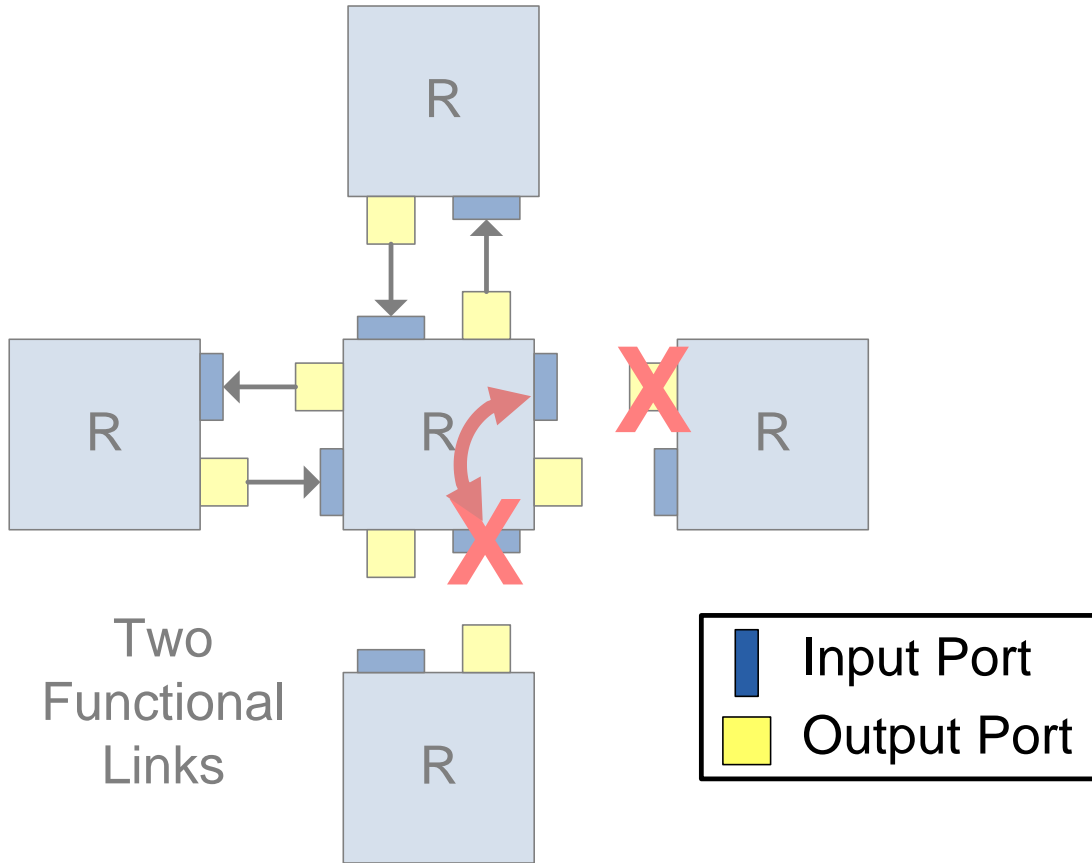


Input Port Swapping

- Partial crossbar gives multiple connection options
- Priority given to local port in order to increase # of available IPs

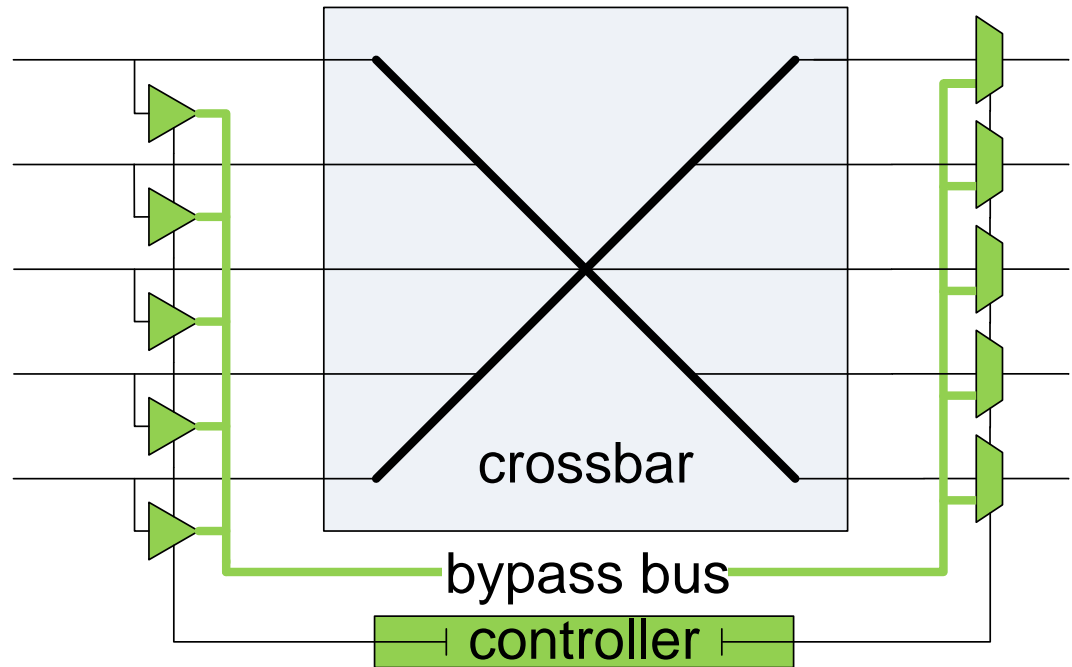


Input Port Swapping

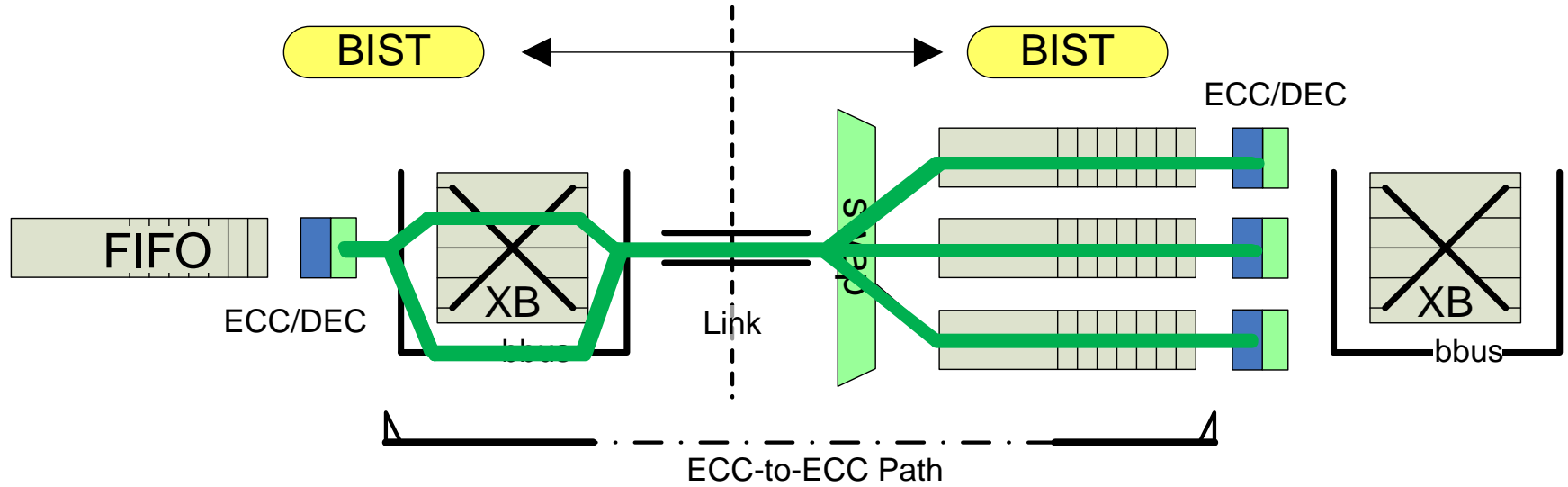


Bypass Bus

- Provides alternative path around crossbar
- Round-robin arbiter inside controller
- No penalty for single user, additional users must stall until free

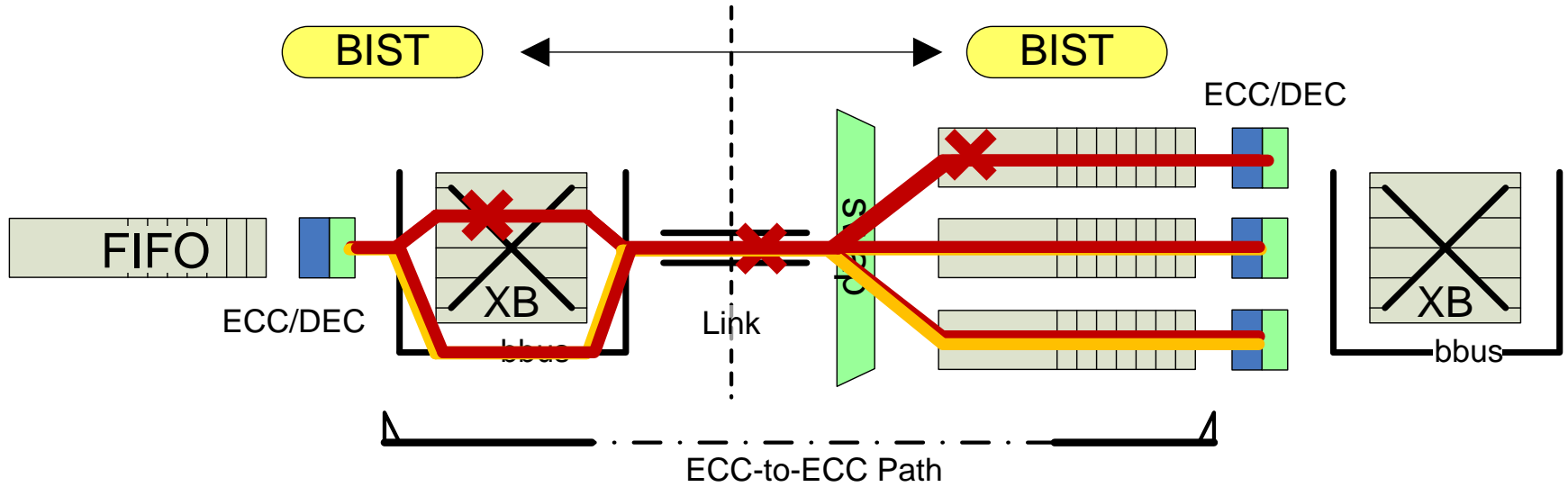


Error Correction Codes



- Six available paths between two routers
- Only one fault may be corrected by ECC
- Fault information for five unit types must be considered:
 - Crossbar, bypass bus, network link, input port swapper, FIFOs
- All configurations must be performed simultaneously
 - Configurations affect each another, network wide

Error Correction Codes

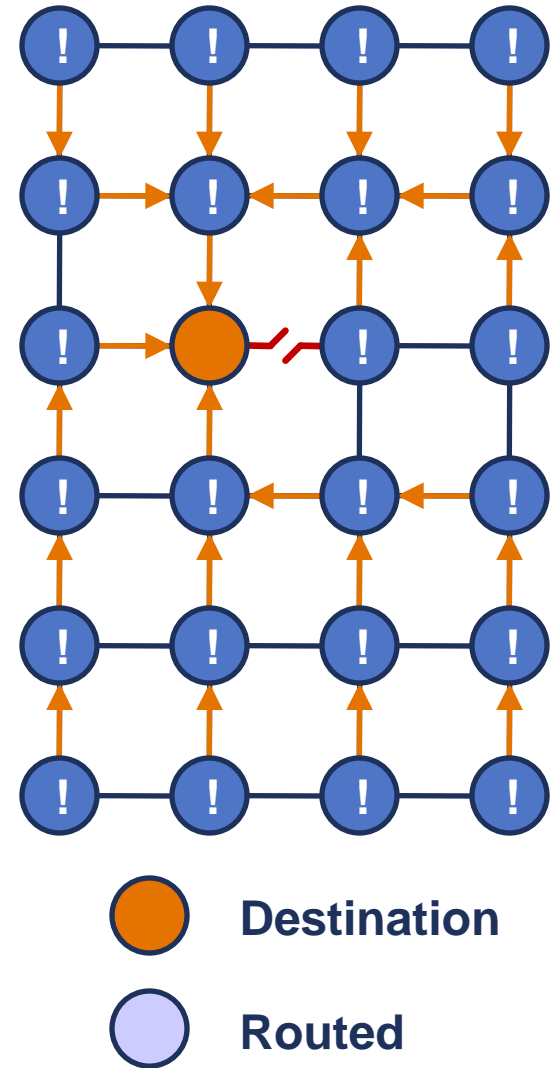


X Single Bit Fault

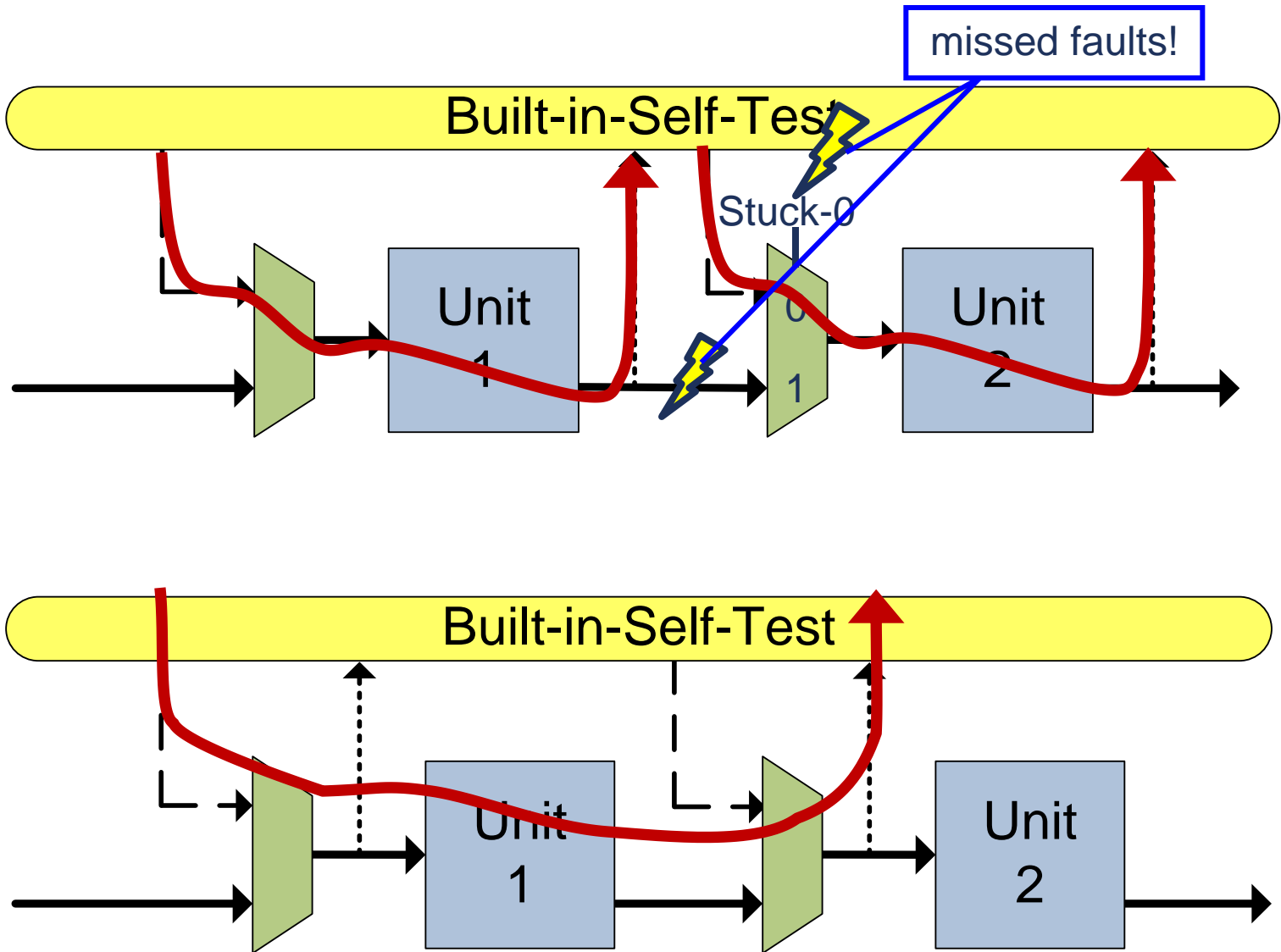
Network Re-routing

[DATE 2009]

- Distributed routing algorithm
- Can route around an arbitrary number of faulty links
- Requires no virtual channels
- Implemented in fewer than 300 gates



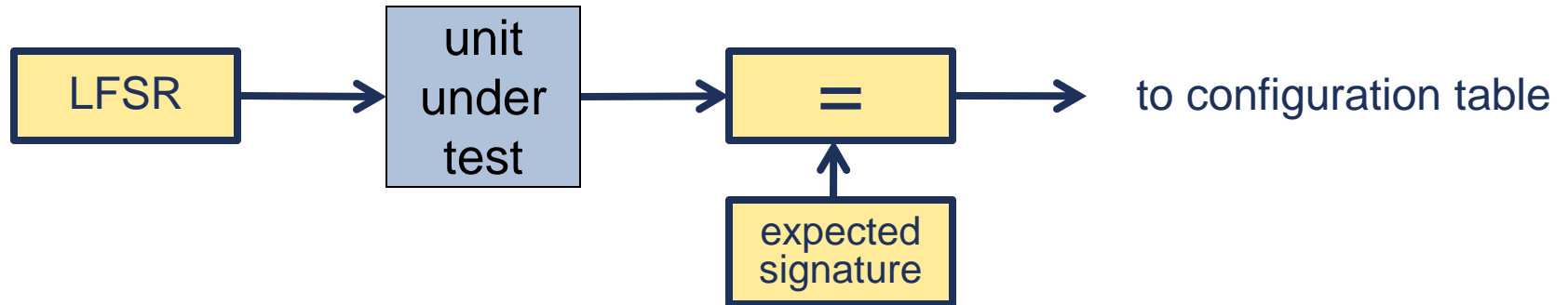
Hard Fault Diagnosis



Hard Fault Diagnosis

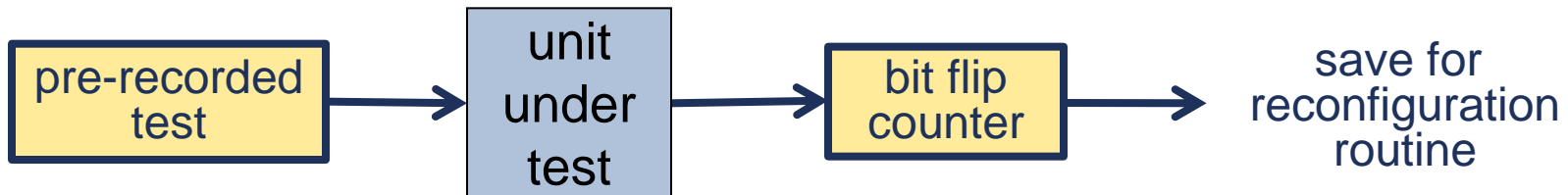
Pattern Based Testing

- Error unit, crossbar controller, routing table, decode/ECC, output ports, FIFO control



Datapath Testing

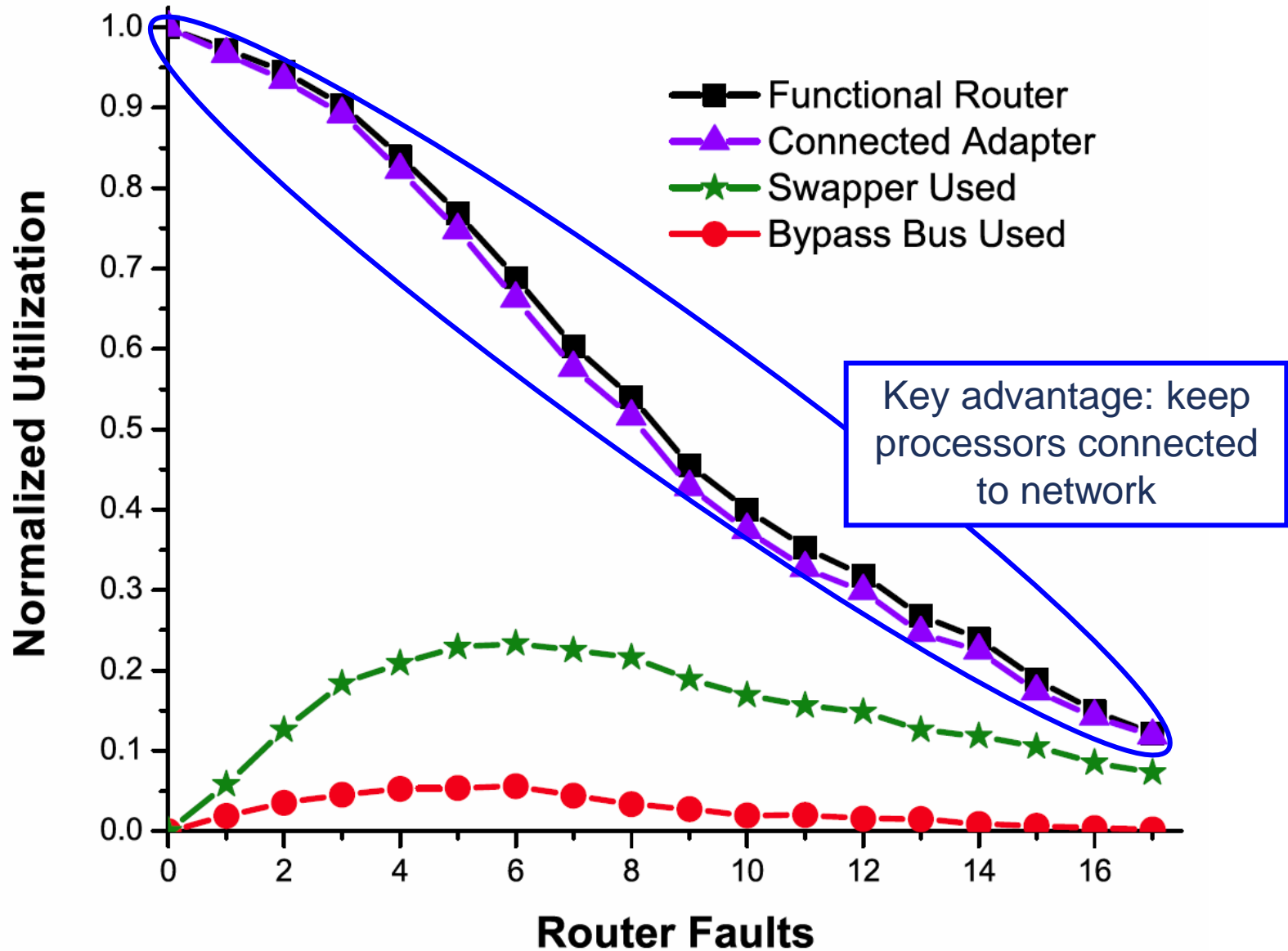
- FIFO datapath, input port swapper, links, crossbar, bypass bus, configuration table



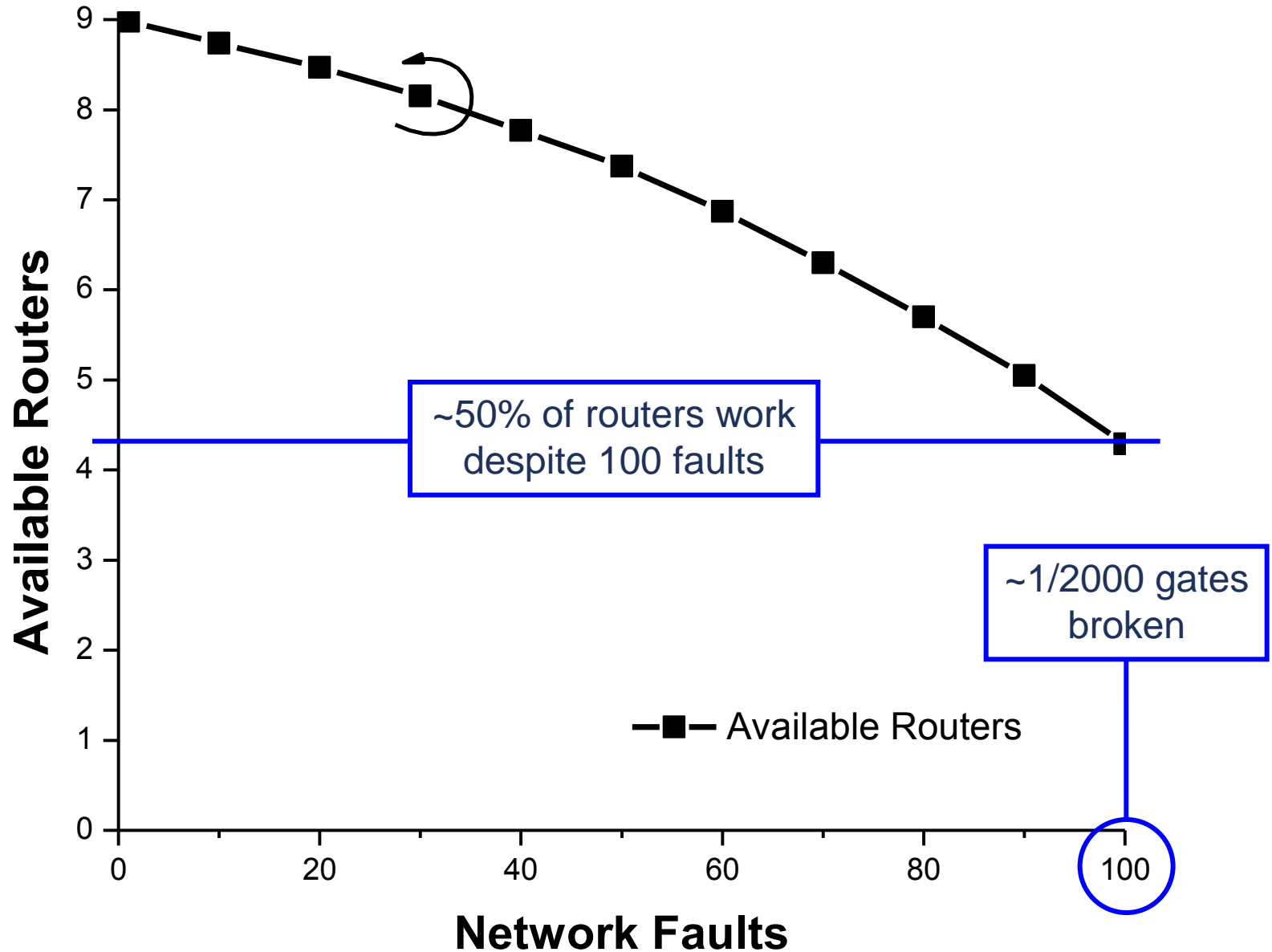
Experimental Setup

- 3x3 Torus
- 32-bit data flits, 32 flit buffers
- Implemented in Verilog
 - Synthesized, automatic place and route in 45nm
 - Reliability results
- Implemented in C++
 - Performance results
- Injected stuck-at faults on gate outputs
 - Weighting based on gate area
- 10,000 packets per test, random uniform traffic
 - Parallel packet injection

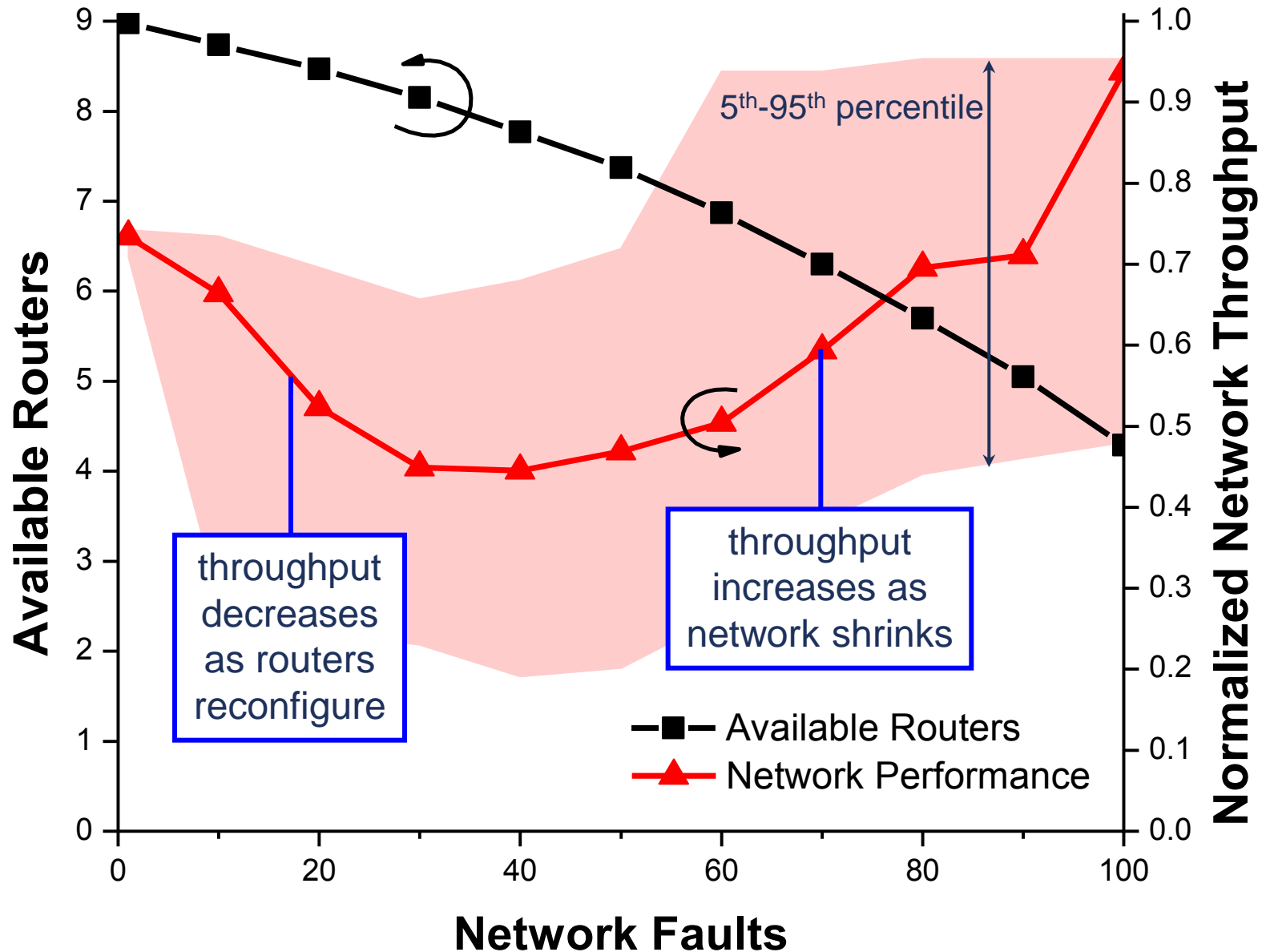
Results – Router Reliability



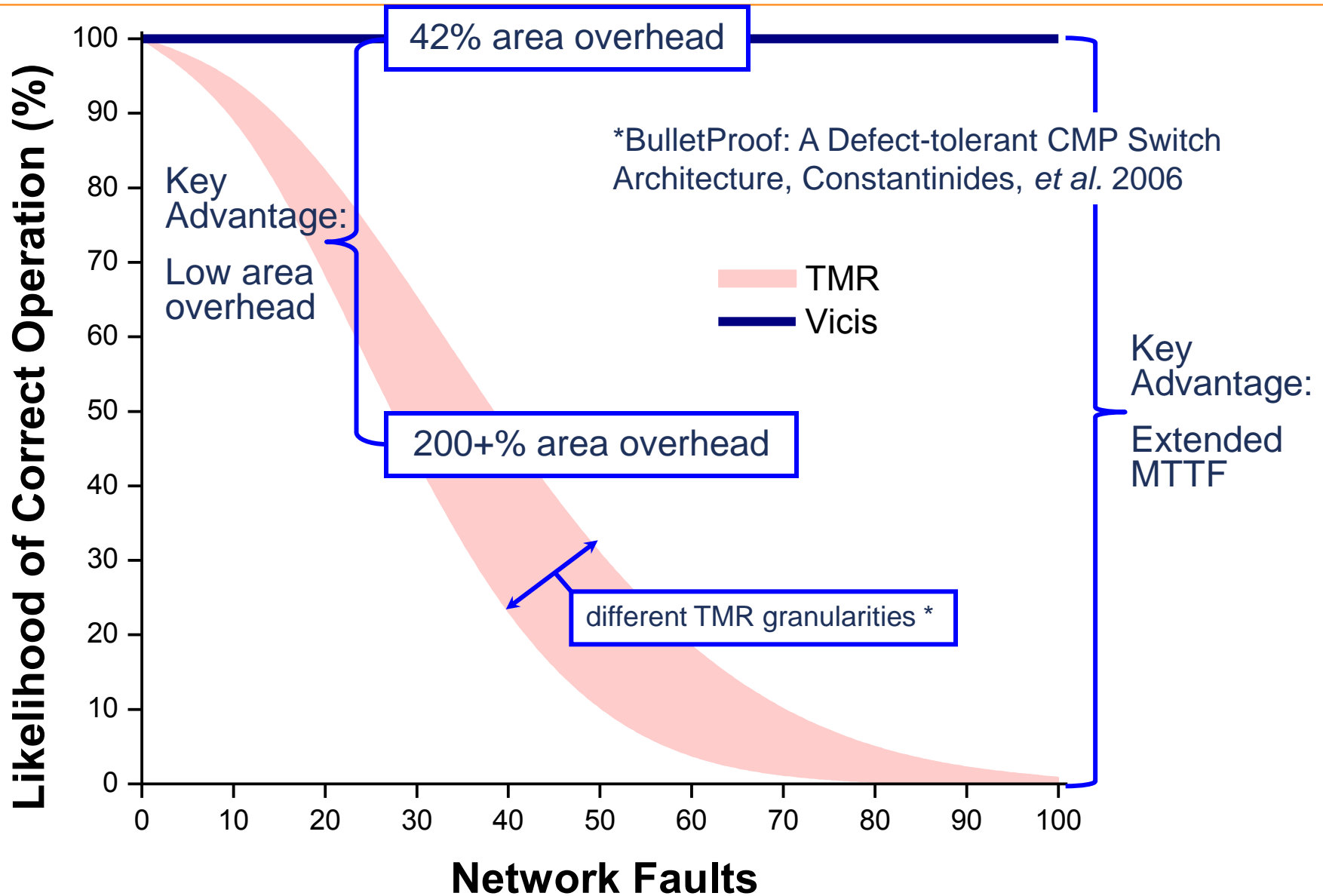
Results – Network Performance



Results – Network Performance



Results – Network Reliability



Conclusion

- Vicis can tolerate a large number of faults
- Vicis provides much greater reliability than NMR based solutions
 - Vicis: constant-reliability, probabilistic performance
 - NMR: constant-performance, probabilistic reliability
- Vicis has an overhead of 42% versus 100+% for NMR